## PENDING CLAIMS AS AMENDED

Please amend the claims as follows:

1. (cancelled)

2. (cancelled)

3. (currently amended) A ~~The~~ system ~~of Claim 2~~ for reducing leakage through an electrical path in an integrated circuit comprising:

a first circuit component in said path between a voltage potential;

a second circuit component in said path; and

means for selectively providing feedback from an output of said second circuit component to an input of said first circuit component to selectively cutoff said path at said first circuit component when said path is not cutoff at said second circuit component, wherein said means for selectively providing feedback further includes means for preserving data in said circuit.

4. (original) The system of Claim 3 wherein said means for preserving data in said circuit includes means for selectively enabling said feedback when said circuit is in sleep mode.

5. (original) The system of Claim 4 wherein said means for selectively enabling said feedback includes a multiplexer.

6. (original) The system of Claim 5 wherein said multiplexer is a 2-1 multiplexer having a shift input as a control input and having a scan-in input as one input and said feedback as a second input.

7. (currently amended) The system of Claim 5 wherein said first circuit component is a first Complementary ~~Complimentary~~ Metal Oxide Semiconductor (CMOS) inverter, and wherein said second circuit component is a second CMOS inverter.

8. (original) The system of Claim 7 wherein said feedback is provided over a feedback path which is chosen so that when said feedback ~~path~~ is enabled ~~activated~~, a high state occurring at an input of said second CMOS inverter results in a high state at an input of said first CMOS

inverter, and a low state occurring at an input of said second CMOS inverter results in a low state at an input of said first CMOS inverter.

9. (currently amended) The system of Claim 7 wherein said integrated circuit is a master-slave latch.

10. (currently amended) The system of Claim 9 wherein when said latch sleeps when a synchronizing clock signal of said latch is high, additional logic shuts off an additional leakage path ~~paths~~ in a master cell of said latch via High Voltage Threshold (HVT) transistors that are positioned in a selectively gated inverter in said master cell.

11. (currently amended) The system of Claim 10 further including means for selectively disabling said feedback when said clock signal sleeps high, and wherein said additional logic is positioned to block said additional leakage path ~~any remaining unblocked leakage paths~~.

12. (currently amended) The system of Claim 11 wherein said ~~further including~~ means for selectively blocking said path ~~via said clock signal and~~ involves an HVT pass gate positioned between said first circuit component and said second component when said clock signal sleeps high.

13. (cancelled).

14. (currently amended) A ~~The~~ latch ~~of Claim 13 wherein said circuit contains~~ comprising:

a clock signal;

a circuit containing LVT and HVT transistors~~, and wherein said~~ arranged so that data is selectively transferred from an input of said latch to an output of said latch in response to said clock signal; and

means for employing feedback within said circuit ~~includes means for blocking~~ to block leakage paths through one of said LVT transistors in said circuit via one or more of said HVT transistors when said circuit is in sleep mode.

15. (original) The latch of Claim 14 wherein said LVT transistors are arranged to minimize setup time and transition delay of said latch when said latch is in operating mode.

16. (currently amended) The latch of Claim 15 wherein said means for employing feedback blocks ~~blocking~~ leakage paths by ~~includes means for~~ turning off said one or more of said HVT transistors when said circuit is in the sleep mode.

17. (currently amended) The latch of Claim 16 wherein said circuit includes a master cell and a slave cell, said feedback occurring from said slave cell to said master cell.

18. (original) The latch of Claim 17 wherein said feedback represents half-latch data from said slave cell.

19. (currently amended) The latch of Claim 18 further including a shift signal, said shift signal indicating when said circuit is in sleep mode.

20. (original) The latch of Claim 15 wherein said latch lacks HVT pass gates in a data path from said input to said output and includes two LVT pass gates in said data path.

21. (original) The latch of Claim 20 wherein one of said LVT pass gates is included in a master cell of said latch, and a second LVT pass gate is included in a slave cell of said latch.

22. (currently amended) The latch of Claim 21 wherein ~~all~~ the leakage paths of said latch flow through off HVT transistors when said latch is in sleep mode.

23. (original) The latch of Claim 22 further including means for automatically enabling said latch to sleep when said clock signal of said latch is high or low.

24. (currently amended) The latch ~~system~~ of Claim 23 wherein when said latch sleeps when said clock signal is high, additional logic shuts off another leakage path ~~paths~~ in said master cell via said HVT transistors that are positioned in a selectively gated inverter in said master cell.

25. (currently amended) The latch ~~system~~ of Claim 24 further including means for selectively disabling said feedback when said clock signal sleeps high, and wherein said additional logic is positioned to block said additional ~~any remaining unblocked~~ leakage path ~~paths~~.

26. (original) The latch of Claim 23 wherein said means for automatically enabling includes a multiplexer in communication with a controller for selectively controlling said feedback.

27. (original) The latch of Claim 26 wherein said multiplexer is integrated with said master cell.

28. (original) The latch of Claim 23 wherein said synchronizing clock signal includes two synchronizing clock signals having different phases.

29. (currently amended) A ~~high-performance, low-leakage~~ latch comprising:

a circuit containing LVT and HVT transistors arranged so that data is selectively transferred from an input of said circuit to an output of said circuit in response to a clock signal, said circuit having LVT pass gates but lacking HVT pass gates in a data path between an input and an output of said circuit; and

means for employing feedback within said circuit to block leakage paths through said LVT transistors via one or more of said HVT transistors when said circuit is in sleep mode by selectively turning off said one or more of said HVT transistors in response to said feedback.

30. (currently amended) A method for reducing current leakage in a circuit comprising ~~the steps of positioning~~ a first circuit component in a path between a ~~relatively high voltage and a relatively low~~ voltage potential, and~~; placing~~ a second circuit component in said path, the method comprising:~~; and~~

selectively providing feedback from an output of said second circuit component to an input of said first circuit component to selectively cutoff said path at said first circuit component when said path is not cutoff at said second circuit component, while preserving data in said circuit.